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IoTGen: Towards LLM-Driven IoT Hardware PCB Generation

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Microsoft Research

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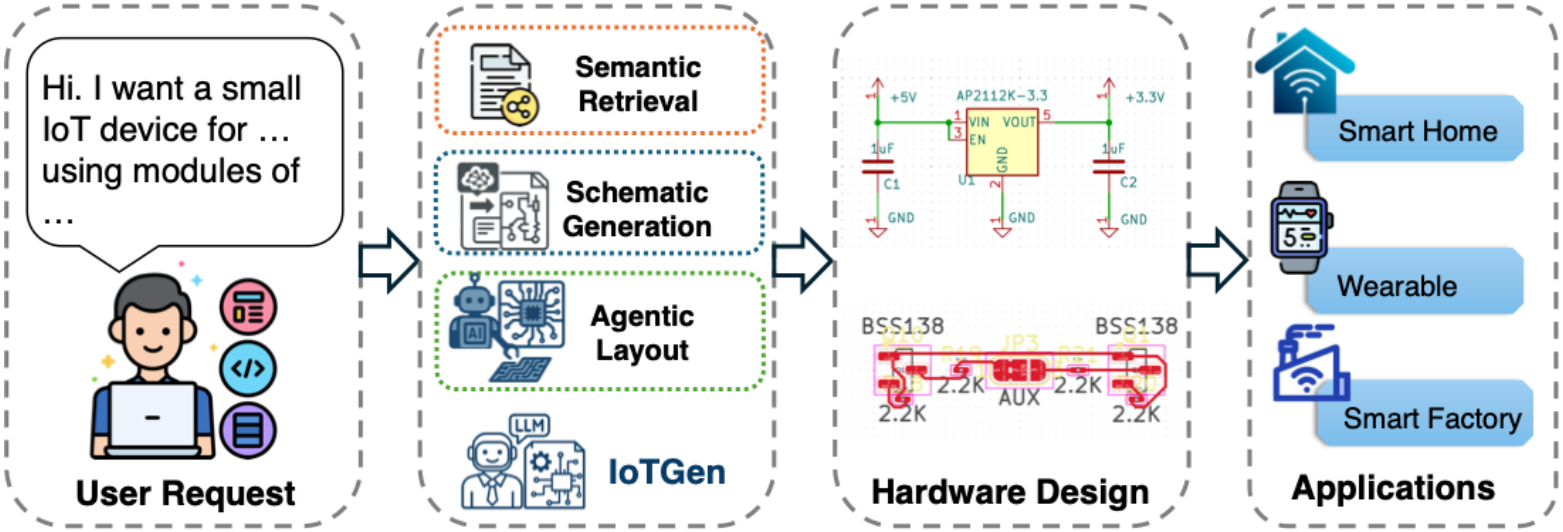
Introduction



- With the growing demand for Internet of Things devices, the need for customized hardware solutions is increasing rapidly
- IoT devices in particular require frequent hardware customization.

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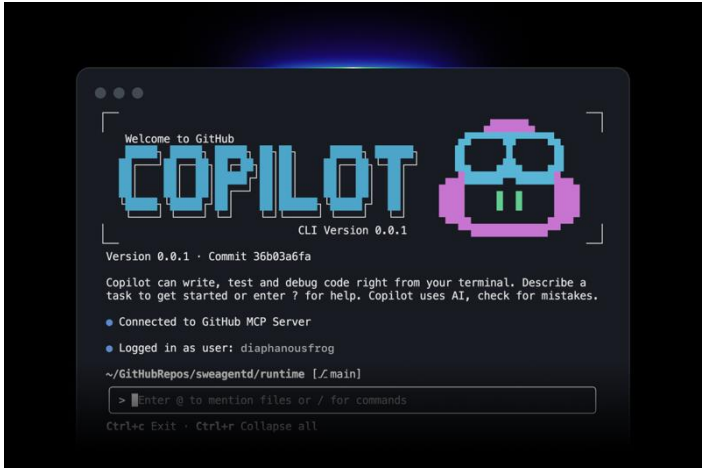
Challenges



1. A significant gap between a design requirement and fabrication-ready PCB designs.
2. Today's IoT PCB design workflow is still GUI-centric and manual, demanding substantial domain expertise.

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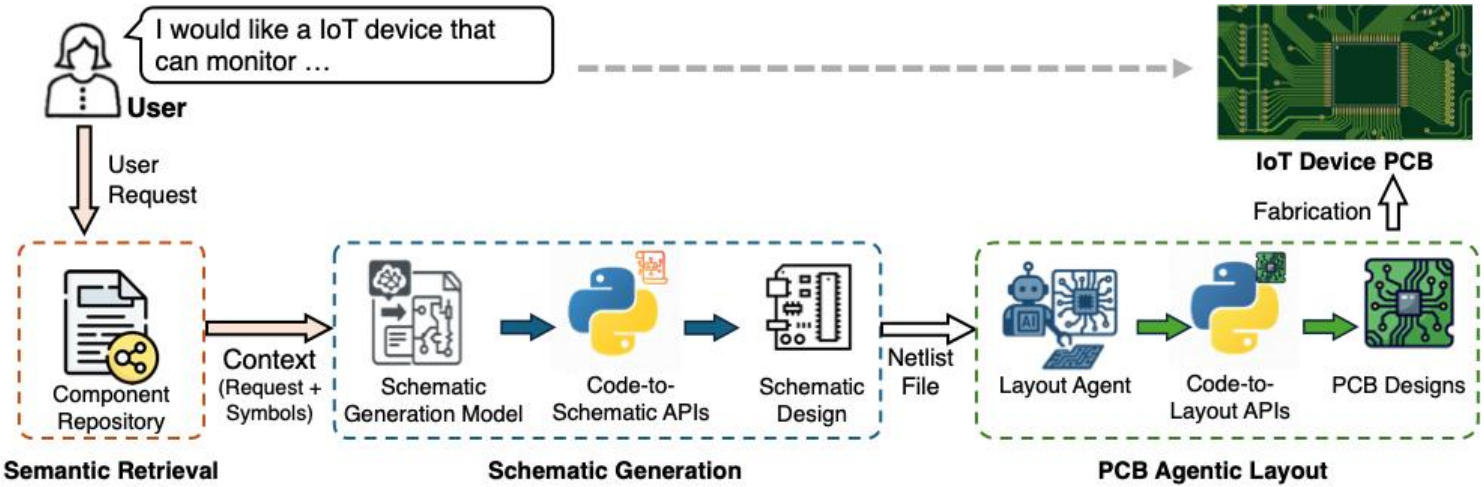
System Design

Overview



- General PCB design pipeline: Schematic→ Netlist→ Layout/Wiring→ Fab
- Schematic File: Component + Power + Net Label + Connection
- PCB Design File: Footprint + Metal Wires + Via holes

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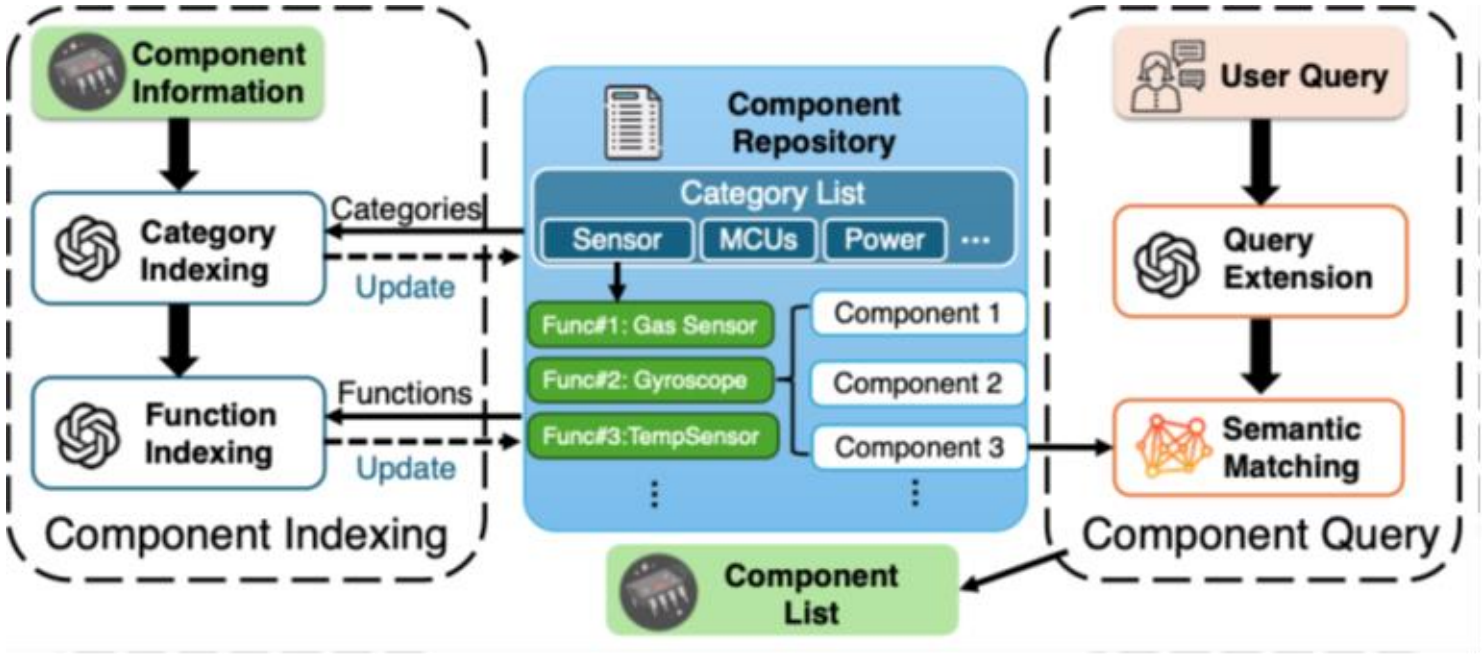
System Design

Semantic Retrieval



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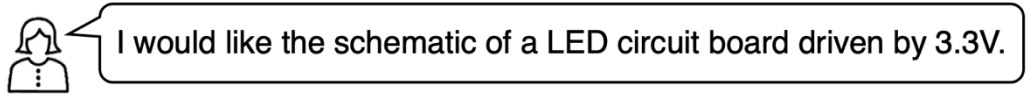
System Design

Code Representation for schematic generation



LLM

```
(kicad_sch
(version 20231120)
(generator "eeschema")
(generator_version "8.0")
(paper "A4")
(lib_symbols
(symbol "Device:R"
(pin_numbers hide)
(pin_names …
```

Text Representation

❌ Uninterpretable
❌ Format Error

LLM + Image Generation

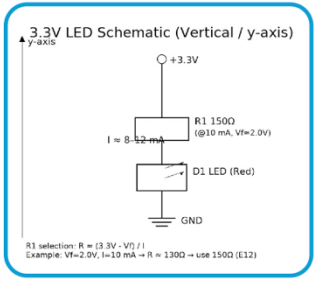
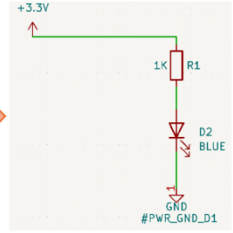


Image Representation

❌ Unsupported Format
❌ Prone to Error

```
add_schematic_symbol(
symbol_lib="Device",
symbol_name="LED",…)
…
connect_pins("D2", "K",
"#PWR_GND_D1", "")
```



Code Representation

✅ Readable and Robust
✅ Suitable for LLM-based generation

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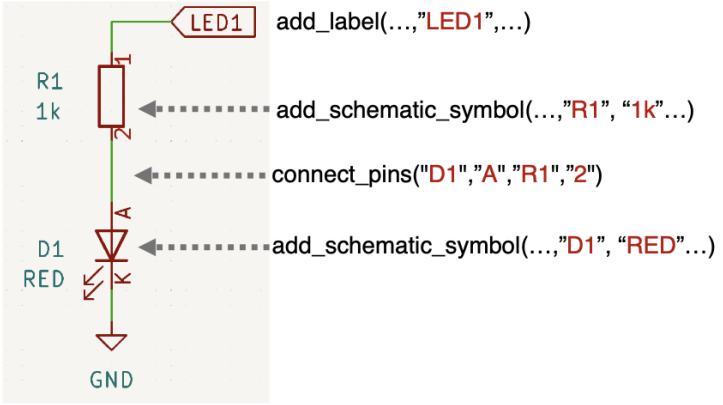
System Design

Code Representation for schematic generation

- Inspired by the observation of human engineers, we represent the schematic with functions called.
- Design Logic:
  - First, put the central symbol.
  - Second, other symbols and labels
  - Finally, connections
- Key Observations:
  - A series of editing operations
  - Placement regarding a local reference/coordinates




```
def add_schematic_symbol(symbol_lib, symbol_name, x, y, ref, value, rotation, mirror):
def add_label(label_pos, label_text, label_ref, label_type, text_orient):
def get_pin_location(symbol_reference, pin_name):
def connect_pins(symbol_ref_a, pin_name_a, symbol_ref_b, pin_name_b):
def write_out_all_wires():
```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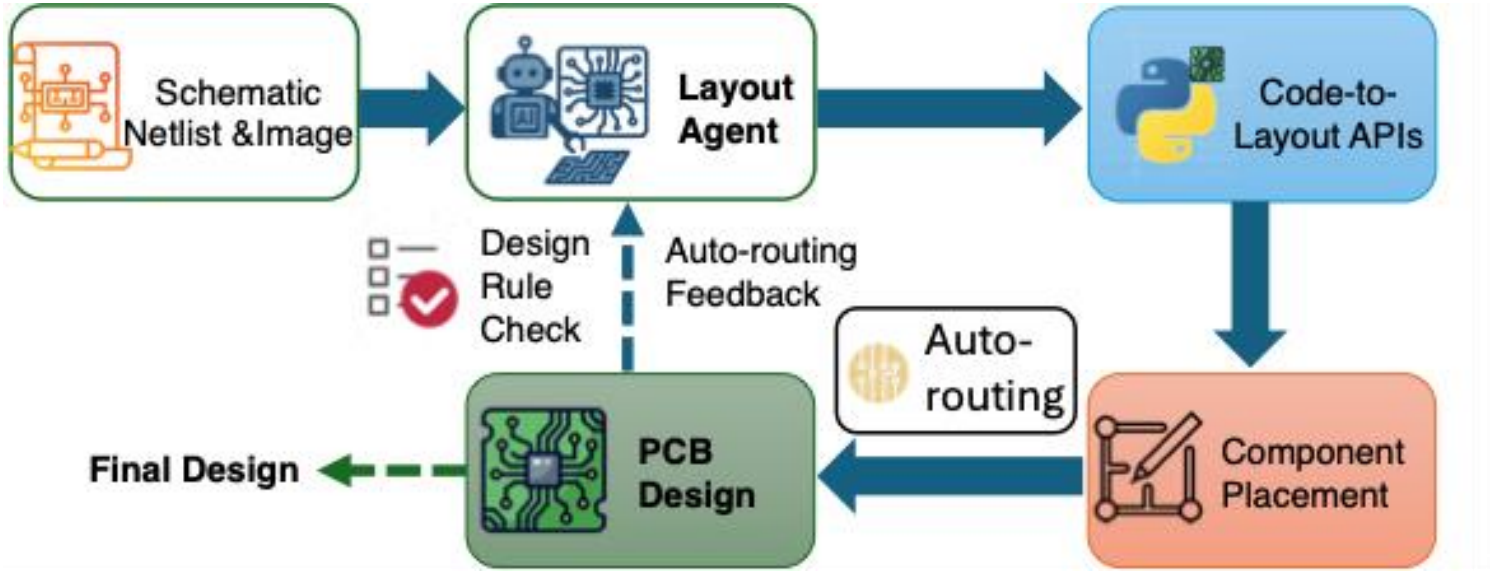
System Design

Agentic Layout



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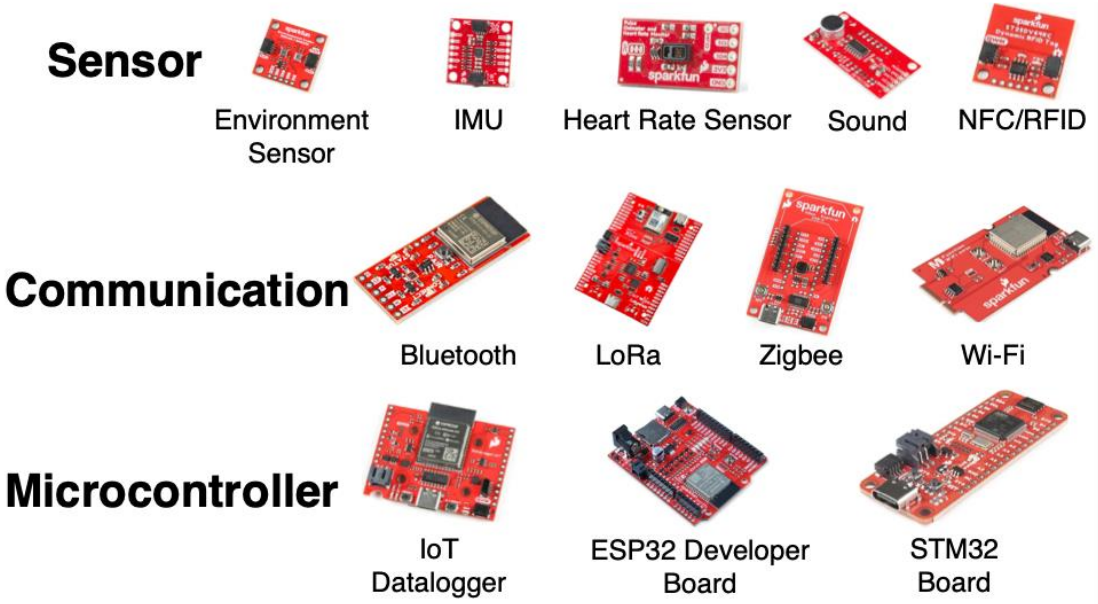
Evaluation

Dataset and Setup



- Dataset: 196 KiCAD full-device schematic designs, spanning various types of functionality, covering microcontroller, analog modules, LED, power, storage, battery, antenna, USB, etc.
- We finetune the base model of *GPT-oss-20b* with LoRA on a single 80 GB Nvidia A100 GPU for schematic generation.
- For the semantic symbol retrieval and agentic PCB layout, we adopt commercial LLM access.

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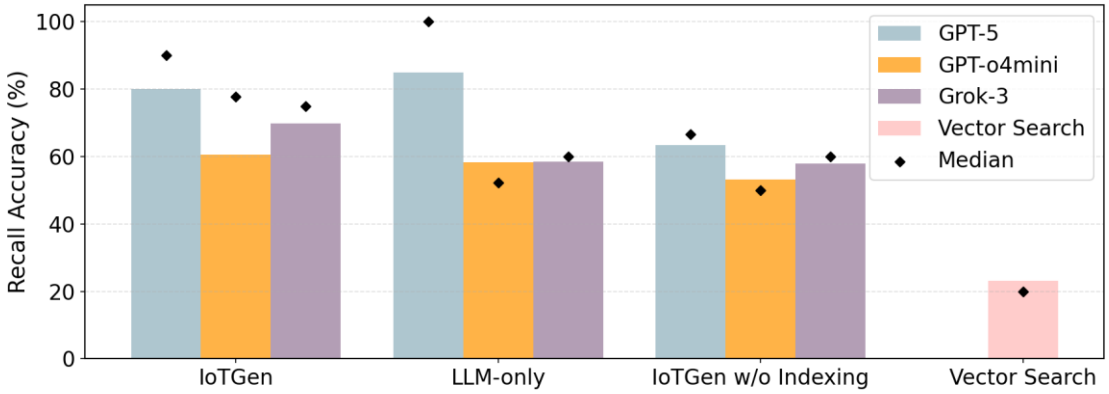
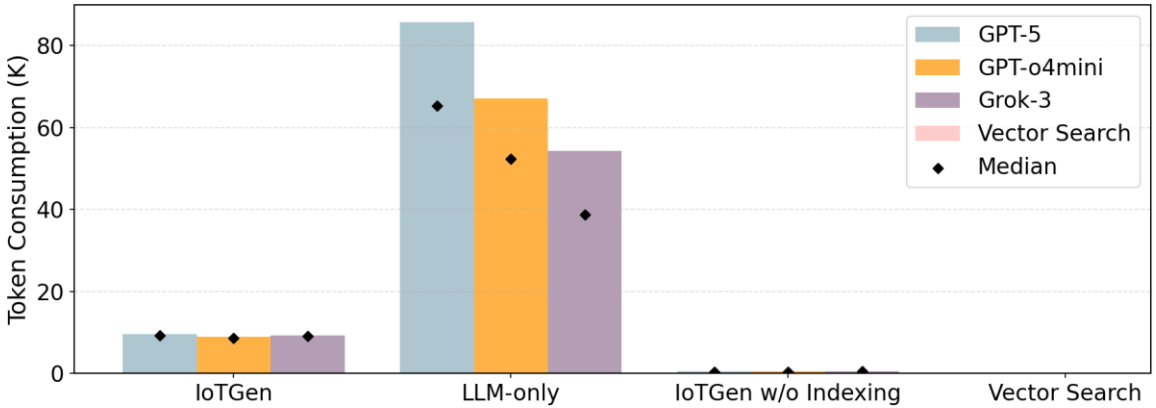
Evaluation

Semantic Retrieval





90% accuracy with only 10% token consumption compared to LLM-only

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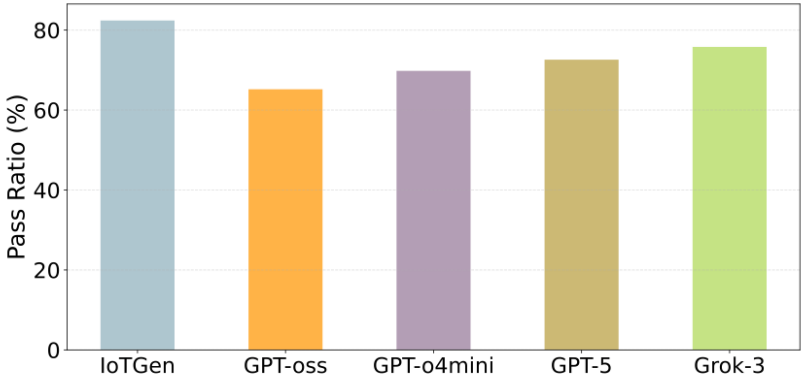
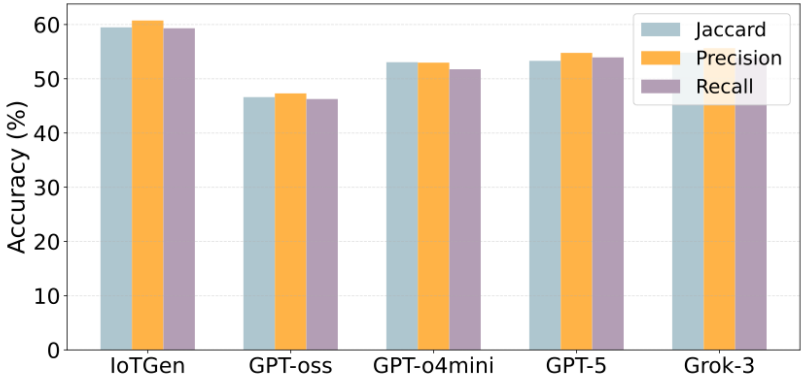
Evaluation

Schematic Generation

- IoTGen outperforms other models regarding ratio of valid circuits and netlist accuracy.
- IoTGen contains a much smaller model compared to those by commercial services.





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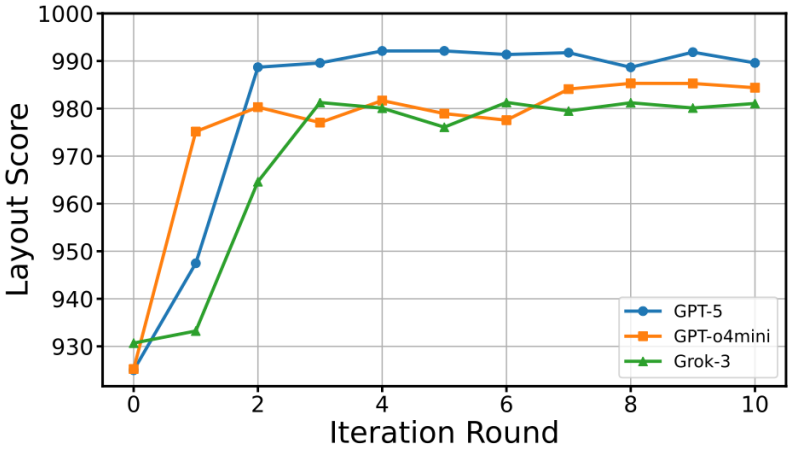
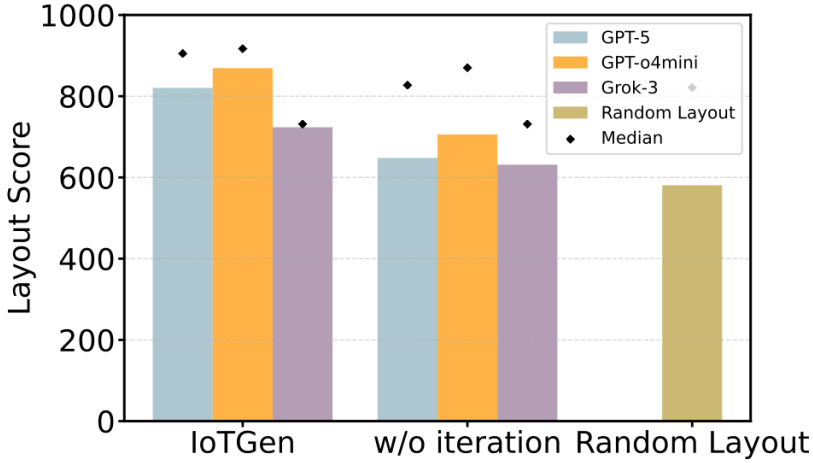
Agentic Layout





- GPT-5 is the best model for iterative agentic layout.
- IoTGen outperforms other two microbenchmarks.

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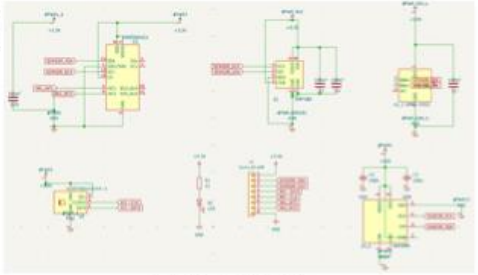
Evaluation

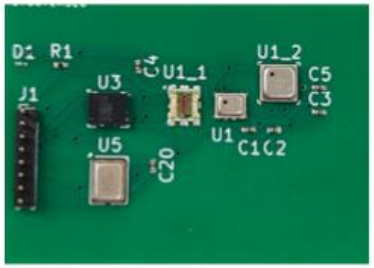
Case Study

(i)



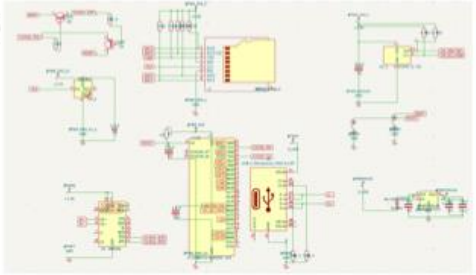
(a) Schematic

(b) PCB Layout

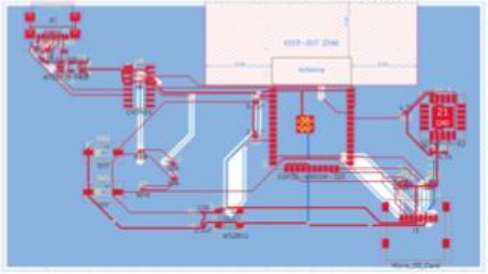


(c) Fabricated PCB

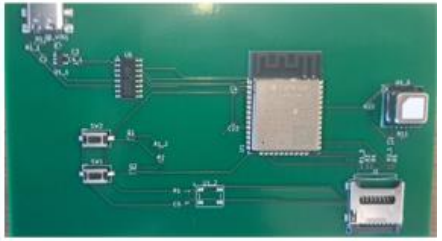
(ii)



(d) Schematic



(e) PCB Layout



(f) Fabricated PCB

Top: Sensor Module
Bottom: CO2 Monitor

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Conclusion

- IoTGen automates the end-to-end PCB design workflow, translating natural-language intent into fabrication-ready IoT hardware.
- It integrates semantic component retrieval, schematic generation, and agentic PCB layout in a unified framework.
- For more details, please check our paper. Our codebase, model and dataset are available at: https://github.com/luoqinpei/IoTGen.git

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